WHAT IS CLAIMED IS:

1. A method for use with a design layout, said method comprising the steps of:

creating a patch cell for a given cell of the layout, said patch cell including at least some features from higher level cells above the given cell, and further including at least some features from the given cell;

identifying instances of a layout deficiency in the patch cell;

adding features to the patch cell to correct one or more of the identified instances;

removing all but the added features from the patch cell; and then

instantiating the patch cell into the layout to thereby effectuate the patch cell corrections into the layout.

2. The method of claim 1 wherein the given cell comprises a cluster cell.

3. The method of claim 1 wherein the patch cell includes metal and via features from higher level cells above the given cell.

4. The method of claim 1 wherein the patch cell includes metal and via features from the given cell.

5. The method of claim 1 wherein the patch cell includes an instantiation of the given cell.

6. The method of claim 1 wherein the added features comprise metal features.

7. The method of claim 6 wherein the added features further comprise via features.

8. The method of claim 1 further comprising flagging any identified instances which remain uncorrected.

9. The method of claim 1 wherein the patch cell is instantiated into the given cell.

10. The method of claim 1 wherein the patch cell is instantiated into the layout at a level above the given cell.

11. The method of claim 1 further comprising creating a respective patch cell for each respective cell at a given level of the layout, and carrying out the enumerated steps for each respective patch cell.

12. The method of claim 1 wherein the identifying step comprises identifying isolated vias.

13. The method of claim 12 wherein the adding step comprises adding dummy metal features within landing areas containing one or more identified isolated vias.

14. The method of claim 12 wherein the adding step comprises adding additional vias.

15. The method of claim 13 wherein the adding step further comprises processing the dummy metal features to ensure compliance with design rule checks (DRC) and electrical rule checks (ERC).

16. The method of claim 15 wherein the adding step further comprises joining covering metal features associated with a single electrical node by at least one of said dummy metal features within a landing area containing one or more identified isolated vias.

17. The method of claim 16 further comprising the steps of:
identifying isolated vias remaining after performing the adding step; and
adding via fill arrays within eligible via fill areas associated with identified isolated vias.

18. The method of claim 17 further comprising flagging any isolated vias remaining after performing the adding via fill arrays step.

19. The method of claim 1 wherein a representation of the design layout is encoded in one or more design files for an electronic circuit.

20. An electronic circuit fabricated from a design layout representation thereof, said design layout being generated by the method recited in claim 1.

21. A method for correcting an existing design layout, said method comprising the steps of:

creating a patch cell for a cluster cell of the layout, said patch cell including covering metal features from higher level cells above the cluster cell, and further including metal and via features from the cluster cell;

identifying isolated vias in the patch cell layout;

adding dummy metal features to the patch cell within landing areas containing one or more identified isolated vias; then

identifying remaining isolated vias in the patch cell layout;

adding via fill arrays within landing areas containing one or more identified isolated vias;

removing all but the added features from the patch cell;

flagging any identified instances which remain uncorrected; and then

instantiating the patch cell into the layout to thereby effectuate the patch cell corrections into the layout.

22. The method of claim 21 wherein the patch cell creating step includes instantiating the cluster cell into the patch cell.

23. The method of claim 21 wherein the patch cell creating step includes copying metal features from upper-level cells above the cluster cell, transforming coordinates and orientation of said copied metal features if different than the patch cell, and including said transformed features into the patch cell as covering metal features.

24. The method of claim 21 wherein the patch cell instantiating step comprises instantiating the patch cell into the cluster cell.

25. The method of claim 21 wherein the patch cell instantiating step comprises instantiating the patch cell into the layout at a level above the cluster cell.

26. The method of claim 21 further comprising repeating the enumerated steps for each respective cluster cell in the layout.

27. The method of claim 21 wherein the dummy metal features adding step further comprises:

processing the dummy metal features to ensure compliance with design rule checks (DRC) and electrical rule checks (ERC) relative to existing metal features and to other dummy metal features, and joining covering metal features associated with a single electrical node by at least one of said dummy metal features within a landing area containing one or more identified isolated vias.

28. A method of making a computer readable media product that encodes a design file representation of a design layout of an electronic circuit, said method comprising the steps of:

creating a patch cell for a given cell of the layout, said patch cell including at least some features from higher level cells above the given cell, and further including at least some features from the given cell;

identifying instances of a layout deficiency in the patch cell;

adding features to the patch cell to correct one or more of the identified instances;

removing all but the added features from the patch cell; and then

instantiating the patch cell into the layout to thereby effectuate the patch cell corrections into the layout; and

encoding the design layout into a computer readable medium.

29. The method of claim 28 wherein the patch cell includes metal and via features from the given cell.

30. The method of claim 28 wherein the added features comprise metal and via features.

31. The method of claim 28 wherein the identifying step comprises identifying isolated vias.

32. A computer readable encoding of an electronic circuit design, the computer readable encoding comprising:

one or more design file media encoding representations of a design layout for the electronic circuit design;

wherein the computer readable encoding of the electronic circuit design was generated by the steps of:

creating a patch cell for a given cell of the layout, said patch cell including at least some features from higher level cells above the given cell, and further including at least some features from the given cell;

identifying instances of a layout deficiency in the patch cell;

adding features to the patch cell to correct one or more of the identified instances;

removing all but the added features from the patch cell; and then

instantiating the patch cell into the layout to thereby effectuate the patch cell corrections into the layout.

33. The computer readable encoding of claim 32 wherein the patch cell includes metal and via features from the given cell.

34. The computer readable encoding of claim 32 wherein the added features comprise metal and via features.

35. The computer readable encoding of claim 32 wherein the identifying step comprises identifying isolated vias.

36. An apparatus for processing one or more design files for an electronic circuit, the one or more design files encoding representations of a design layout of the

electronic circuit, said design layout having vias connecting geometries of a first layer to geometries of a second layer, said apparatus comprising:

means for creating a patch cell for a given cell of the layout, said patch cell including at least some features from higher level cells above the given cell, and further including at least some features from the given cell;

means for identifying instances of a layout deficiency in the patch cell;

means for adding features to the patch cell to correct one or more of the identified instances;

means for removing all but the added features from the patch cell; and

means for instantiating the patch cell into the layout to thereby effectuate the patch cell corrections into the layout.

37. The apparatus of claim 36 wherein the patch cell includes metal and via features from the given cell.

38. The apparatus of claim 36 wherein the added features comprise metal and via features.

39. The apparatus of claim 36 wherein the identifying step comprises identifying isolated vias.

40. A computer readable encoding of instructions for a computer, said instructions encoding a method for use with a design layout, for identifying and correcting instances of a layout deficiency within the design layout, said encoded method comprising the steps of:

creating a patch cell for a given cell of the layout, said patch cell including at least some features from higher level cells above the given cell, and further including at least some features from the given cell;

identifying instances of a layout deficiency in the patch cell;

adding features to the patch cell to correct one or more of the identified instances;

removing all but the added features from the patch cell; and then

instantiating the patch cell into the layout to thereby effectuate the patch cell corrections into the layout.

41. The computer readable encoding of claim 40 wherein the patch cell includes metal and via features from the given cell.

42. The computer readable encoding of claim 40 wherein the added features comprise metal and via features.

43. The computer readable encoding of claim 40 wherein the identifying step comprises identifying isolated vias.